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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,181	12/07/2004	Johannes Wilhelmus Theodorus Eikenbroek	P15069-US1	5687

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ERICSSON INC.
6300 LEGACY DRIVE
M/S EVR 1-C-11
PLANO, TX 75024

EXAMINER	
ANYIKIRE, CHIKAODILI E	
ART UNIT	**PAPER NUMBER**
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/26/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,181	EIKENBROEK, JOHANNES WILHELMUS THEODORU	
	Examiner	Art Unit	
	Chikaodili E. Anyikire	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-19* is/are rejected.

7)☒ Claim(s) *8,12, and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application is responsive to application number (10/517, 181) filed on December 10, 2004. Claims 1-14 and 17-19 are pending and have been examined.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. (10/517, 181), filed on 12/7/2004.

Preliminary Amendment

3. Acknowledgement of the applicant's preliminary amendment for Application No. (10/517, 181), filed on 12/7/2004.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

4. The disclosure is objected to because of the following informalities: (Page 9, first paragraph, line 3). The statement: "An output of the second combine" should be deleted since on line 4, this statement seems to be repeated

Appropriate correction is required.

Claim Objections

5. Claim 13 objected to because of the following informalities: lacks clarity and precision. In line 2, applicant states with a zero comprises and line 5 states further comprising; all these components of the device in the claim appear to be of equal weighting and therefore comprises and further comprising division lacks clarity and precision. For the purposes of examination the examiner will omit line 5. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/005805).

As per claim 1, Eriksson et al. teaches a phased locked loop (PLL) circuit (Fig 6) at least including:

A loop input (Fig 6, 601);

A phase detector section (Fig 6, 602) for detecting a phase difference between an input signal (601) and a reference signal (Col 5, Ln 20 – 25),

said phased detector section (602) having a detector input connected to said loop input (601), a reference input and a detector output for outputting a signal related

to said input (601) (Col 5, Ln 20 – 25), a reference input and a detector output for outputting a signal related to said phase difference (Col 5, Ln 20 – 25);

A controlled oscillator (Fig 6, 604) having an input communicatively connected to said detector output (Col 5, 25 – 27) and an oscillator output connected to a loop output (Fig 6, 605, figure 6 shows the connection between the oscillator (604) and the loop output (605); and

A feed back circuit connecting said oscillator output to said reference input (Col 5, Ln 26 – 29).

Eriksson et al teaches a feedback circuit, but does not explicitly teach a device having a transfer function with at least one zero, and the phase locked loop circuit has a closed loop transfer function without zeros.

However in the same field of endeavor, Sridharan teaches a feedback circuit (Fig 8) includes a device having a transfer function with at least one zero (Fig 8, 819, [0027]), and the phase locked loop circuit has a closed loop transfer without zeros (Fig 8, the applicant should note that there is no zero in the forward path of the closed loop circuit and that when closed loop equation is used with this circuit

$H_{closed}(s) = \frac{H(s)}{1 + G(s)H(s)}$; where H(s) represents the forward path of Fig 8, which includes the filter (815) and the quantizer (817) and G(s) represents the feedback path which includes the second filter (819) and that there are no zeros in the closed loop transfer function of the zero either).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine "Fractional-N Type Frequency Synthesizer"

figure of Sridharan (Fig 8) and "Compensated ΔΣ Controlled Phased Locked Loop modulator" phased locked loop of Eriksson to gain stability in the feedback circuit and improve the out-of-band attenuation.

As per claim 2, Eriksson teaches the phase locked loop circuit as claimed in claim 1 further including a filter section (603) having a filter input connected to said detector output and a filter output connected to said oscillator input (Col 5, Ln 25 – 28).

As per claim 3, Eriksson teaches the phase locked loop circuit as claimed in claim 1 said feedback circuit further includes at least one frequency divider device (Fig 6, 606).

As per claim 4, Eriksson teaches wherein said frequency divider device (606) is connected to a delta-sigma modulator (Fig 6, 610).

As per claim 5, Eriksson teaches a frequency divider device (606), but does not explicitly teach a frequency divider device that has a transfer function with said zero.

However in the same field of endeavor, Sridharan teaches a device with a transfer function with zero (Sridharan, Fig 8, 819, [0027]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the frequency divider device of Eriksson with a transfer function with at least one zero, from Sridharan. The advantages to the

integration of these two components to the system are that it would have provided stability to the phase locked loop and improved the out-of-band attenuation.

9. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/0058055), as applied to claim 3 above, and further in view of Liang et al. (US 5, 550, 515).

As per claim 6, the device of Eriksson et al. as modified by Sridharan teach wherein said feedback circuit includes a second frequency divider having a transfer function with a zero (see rejection of claim 5 and Sridharan in Fig 8, 819), but does not teach a first frequency divider device.

However, Liang et al. teaches a secondary frequency divider device (Fig 2, 109). Liang teaches multiple frequency dividers in parallel in the feedback loop to produce multiple error signals between the frequency divider signals and reference signal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the device having a transfer function with a zero as taught by the modified device of Eriksson with the second frequency divider device (Liang et al., Fig 2, 109). The integration of the device having a transfer function with a zero and the second frequency divider device would provide more control over the division ratio by having multiple dividers for the frequency outputted at the VCO of the modified device.

10. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/0058055) in view of Liang et al. (US 5, 550, 515), as applied to claim 6 above, and further in view of Perrett et al. (US 6, 018, 275).

As per claim 7, the device of Eriksson et al as modified by Sridharan and Liang teaches wherein said first and second divider device are connected in parallel (Liang et al, Fig 2, 109).

However, the device of Eriksson as modified by Sridharan and Liang does not explicitly teach wherein an output of the first frequency each connected to an input of a second combiner device, and wherein an output of the second combiner device is connected to the reference input of the phase detector section.

However in the same field of endeavor, Perrett et al. teaches a PLL (30) comprising a modulator (34) in the feedback path. Perrett et al. further teaches the output of the first frequency divider device and an output of the second frequency divider device is connected to an first input of a second combiner device (Fig 4, 39) which is connected to the reference input of the phase detector section (Perrett, Col 6, Ln 5 – 9; the applicant should be aware that the combiner device is too broad and so can be interpreted broadly as a modulator that combines an integrator and phase modulator such as the prior art used).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the feedback loop of Eriksson as modified by Sridharan and Liang with the modulator of Perrett et al. The addition of the modulator of

Perrett et al provides extra processes of the signal from the modified device, which will ensure a better signal as the reference signal to the phase detector section of the modified device.

11. Claim 9 and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/0058055) as applied to claim 3 above and in further view of Okumura (US 6, 032, 277).

As per claim 9, the device of Eriksson et al as modified by Sridharan does not teach frequency divider device is connected in series with a device. It should be noted that Sridharan teaches a device having a transfer function with a zero.

In the same field of endeavor, Okumura teaches a frequency divider device is connected in series with a device (Fig 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the feedback loop of the modified device of Eriksson in view of Sridharan with that of Okumura to show a frequency divider device in series with a device having a transfer function with a zero. The integration of the feedback loop of the modified device with that of Okumura with the motivation of keeping the oscillation delayed or advanced while the signal, indicative of a change in oscillation period, reaches the phase comparator (Col 3 Ln 66 – 67 and Col 4, Ln 1).

As per claim 10, the device of Eriksson et al as modified by Sridharan does not teach an input connected to the controlled oscillator and an output connected to an

input of the frequency divider. It should be noted that Sridharan teaches a device having a transfer function with a zero.

However in the same field of endeavor, Okumura teaches an input connected to the controlled oscillator and an output connected to an input of the frequency divider (Fig 10; it can be seen from this figure that the circuit (device) is connected to both the PLL element and the frequency divider; Fig 15 describes the PLL element and shows the VCO device specified in the claim).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the modified device of Eriksson et al with the invention of Okumura with the motivation of keeping the oscillation delayed or advanced while the signal, indicative of a change in oscillation period, reaches the phase comparator (Col 3 Ln 66 – 67 and Col 4, Ln 1).

12. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/0058055) as applied to claim 3 above in further view of Okumura (US 6, 032, 277) and in further view of Perrett (US 6, 018, 275).

As per claim 11, the device of Eriksson et al as modified by Sridharan and Okumura does not teach has an input connected to an output of the frequency divider and an output connected to an input of the phase detector section. It should be noted that Sridharan teaches a device having a transfer function with a zero.

However in the same field of endeavor, Perrett teaches an input connected to an output of the frequency divider and an output connected to an input of the phase detector section (Fig 4, 39, fdiv and fc1; the zero device would replace the modulator or even be combined and the claim specified will be fulfilled).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the feedback loop of Eriksson et al as modified by Sridharan and Okumura with the frequency divider of Perrett modulates the baseband signal (f_{bb}) onto the signal f_{div} output by the main frequency divider and the resultant modulated signal f_{c1} is fed to one of the phase detector inputs. The modulator may comprise an integrator and phase modulator (Fig 4 and 5, Col 6 Ln 3 – 11).

13. Claim 14, 17 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/005805).

As per claim 14, Eriksson et al. teaches a method for generating a periodic signal (Fig 6) comprising the steps of:

receiving a periodic signal of a first frequency (Fig 6, 601);

comparing a phase of said periodic signal (601) with a phase of a reference signal generating a difference signal relating to a phase difference between said periodic signal and said reference signal (Fig 6, 602, Col 5, Ln 20 – 25);

filtering said difference signal (Fig 6, 603);

generating an output signal with a frequency corresponding to an amplitude of said difference signal (Fig 6, 604);

transmitting said output signal further (Fig 6, 605);

generating said reference signal by changing said output signal such that the frequency of the output signal is lowered (Col 5, Ln 26 – 29);

wherein for said changing of said output signal a feedback circuit (Fig, 6, 606).

However Eriksson does not explicitly teach having a transfer function with at least one zero, is used, and said receiving a periodic signal until said transmitting said output signal involves a closed loop transfer function without zeros.

In the same field of endeavor, Sridharan teaches wherein for said changing of said output signal a feedback circuit (Fig 8) having a transfer function with at least one zero (Fig 8, 819), is used, and said receiving a periodic signal until said transmitting said output signal involves a closed loop transfer without zeros (Fig 8, the applicant should note that there is no zero in the forward path of the closed loop circuit and that when closed loop equation is used with this circuit $H_{closed}(s) = \frac{H(s)}{1 + G(s)H(s)}$; where H(s) represents the forward path of Fig 8, which includes the filter (815) and the quantizer (817) and G(s) represents the feedback path which includes the second filter (819) and once the closed loop transfer function is computed there are no zeros in the closed loop transfer function).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine "Fractional-N Type Frequency Synthesizer" figure of Sridharan (Fig 8) and "Compensated ΔΣ Controlled Phased Locked Loop modulator" phased locked loop of Eriksson to gain stability in the feedback circuit and improve the out-of-band attenuation.

As per claim 17, Eriksson teaches the limitation wherein said feedback circuit includes at least one frequency divider device (Fig 6, 606).

As per claim 18, Eriksson teaches a frequency divider device (606), but does not explicitly teach a frequency divider device that has a transfer function with said zero.

However in the same field of endeavor, Sridharan teaches a device with a transfer function with zero (Sridharan, Fig 8, 819, [0027]; it is possible to combine the transfer function from Sridharan with the frequency divider device from Eriksson).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the frequency divider device of Eriksson with a transfer function with at least one zero, from Sridharan. The advantages to the integration of these two components to the system are that it would have provided stability to the phase locked loop and improved the out-of-band attenuation.

14. Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson et al. (US 6,011,815) in view of Sridharan (US 2003/0058055), as applied to claim 17 above, and further in view of Liang et al. (US 5, 550, 515).

As per claim 19, the modified device of Eriksson et al. does not teach a second frequency divider device. It should be noted that Sridharan teaches a device having a transfer function with a zero (Fig 8, 819).

However, Liang et al. teaches a secondary frequency divider device (Fig 2, 109). Liang teaches multiple frequency dividers in parallel in the feedback loop to produce multiple error signals between the frequency divider signals and reference signal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the device having a transfer function with a zero as taught by the modified device of Eriksson with the second frequency divider device (Liang et al., Fig 2, 109). The integration of the device having a transfer function with a zero and the second frequency divider device would provide more control over the division ratio by having multiple dividers for the frequency outputted at the VCO of the modified device.

Allowable Subject Matter

15. Claims 8, 12, and 13 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter:

17. As per claim 8, the prior art or the combination of art of record does not teach: a second frequency divider connected to an first input of a second combiner device, a second input of the second combiner device is connected to the output of the phase detector, an output of the second combiner device is communicatively connected to the VCO, and wherein:

the second divider device comprises a phase detector section and has a transfer function with said zero.

As per claim 12, the prior art or the combination of art of record does not teach: a device having a transfer function with a zero has a first input connected to said delta-sigma modulator and a second input connected to the output of the frequency divider.

As per claim 13, the prior art or the combination of art of record does not teach: a device having a transfer function with a zero comprises:

A device with a transfer function equal to $\tau_s S$, said device with a transfer function equal to $\tau_s S$ with a device input connected to the output of the oscillator,

said device having a transfer function with a zero further comprising:

a combiner device with:

a first combiner input connected to the output of the device with a transfer function equal to $\tau_s S$;

a second combiner input connected to the input of the device with a transfer function equal to $\tau_s S$, and

a combiner output connected to the input of the frequency divider device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chikaodili E. Anyikire whose telephone number is (571) 270 -1445. The examiner can normally be reached on Monday to Friday, 7:30 am to 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 270 - 1455. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CEA

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER